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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,693	03/16/2004	Shinji Ohuchi	KKH.041D2	1770

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EXAMINER	
PIZARRO CRESPO, MARCOS D	
ART UNIT	PAPER NUMBER
2814	
MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/800,693	OHUCHI, SHINJI	
	Examiner	Art Unit	
	Marcos D. Pizarro	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12,14-17,19-22,24-27 and 29-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12,14-17,19-22,24-27 and 29-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Attorney's Docket Number: KKH.041D2

Filing Date: 3/16/2004

Claimed Priority Dates: 6/12/2001 (Divisional of 09/878,375)
2/4/2000 (Divisional of 09/497,684)
2/8/1999 (JP 11-029479)

Applicant(s): Ohuchi

Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment filed on 11/14/2007.

Acknowledgment

1. The amendment filed on 11/14/2007, responding to the Office action mailed on 8/20/2007, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 12, 14-17, 19-22, 24-27, and 29-31.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 12, 14, 15, 17, 19, 20, 22, 24, 25, 27, 29, and 30 are rejected under 35 U.S.C. § 103 (a) as obvious over Elenius in view of Hashimoto (WO98-25297), Matsumoto (JP 05-234972) and Yamada (US6048749).

4. Regarding claim 12, Elenius shows (see, *e.g.*, fig. 2) most aspects of the instant invention including a semiconductor device comprising:

- A semiconductor element **14** having a first surface and a second surface opposite to the first surface
- An electrode **18** formed at the first surface of the semiconductor element
- A wiring portion **30** formed on the first surface and connected to the electrode **18**
- A conductive post (lower portion of **28**) formed on the first surface and connected to the wiring portion **30**
- A resin layer **32** formed on the first surface so as to cover the first surface, the wiring portion **30**, and a side of the conductive post
- An external connection **28** formed on the post
- A protective layer **34** formed on the second surface

Wherein:

- An end portion of the protective layer **34** is aligned with both an end portion of the semiconductor element **14** and an end portion of the resin layer **32**
- The end portions of the protective layer **34**, the semiconductor element **14**, and the resin layer **32** define an outer edge of the device
- The protective layer **34** comprises a hardened synthetic resin achieving a bonding function

3. Regarding claims 14, 19, 24, and 29, Elenius shows the protective layer comprises a polyimide or an epoxy resin (see, *e.g.*, col.8/ll.29).

4. Regarding claims 15, 20, 25, and 30, Elenius shows the external connection is a solder ball (see, *e.g.*, col.6/ll.63).

5. Regarding claim 17, Elenius shows a side surface of the semiconductor element **14** is exposed from the resin layer **32** and the protective layer **34** (see, *e.g.*, fig. 2). See also the comments stated above in paragraph 4 with respect to claim 12, which are considered repeated here.

6. Regarding claim 22, Elenius shows (see, *e.g.*, fig. 2):

- The conductive post (lower portion of **28**) having a first end portion and a second end portion
- The post being formed on the first surface
- The first end portion of the post being connected to the wiring portion **30**
- The second end portion of the post is not covered by the resin layer **32**
- The external connection **28** is formed on the second end portion of the post
- Only a side surface of the semiconductor element **14** is exposed from the resin layer **32** and the protective layer **34**

7. Regarding claim 22, see also the comments stated above in paragraph 4 with respect to claim 12, which are considered repeated here.

8. Regarding claim 27, Elenius shows (see, *e.g.*, fig. 2):

- A side surface of the protective layer **34** is in a same plane with both a side surface of the semiconductor element **14** and a side surface of the resin layer **32**
- The side surfaces of the protective layer **34**, the semiconductor element **14**, and the resin layer **32** define an outer edge of the device

9. Regarding claim 27, see also the comments stated above in paragraph 4 with respect to claim 12, which are considered repeated here.

10. Regarding claims 12, 17, 22, and 27, it is noted that Elenius shows most aspects of the claimed invention. He, however, fails to show that the protective layer is a tape. On the other hand, Elenius' protective layer is a hardened synthetic resin applied by known spin coating processes (see, *e.g.*, col.8/ll.24-37).

11. In a similar device to Elenius, Matsumoto also forms a protective layer on the second surface of a semiconductor element to prevent cracking and chipping (see, *e.g.*, abstract). Said protective layer may be formed by either sticking an adhesive tape or spin coating (see, *e.g.*, paragraph 0015). Although both processes could be used, the protective layer is preferably formed from an adhesive tape to avoid wasting resin material (see, *e.g.*, Hashimoto: pp.12/ll.21-28).

12. Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art to tape the protective layer of Elenius to the second surface of the semiconductor element, as suggested by Matsumoto and Hashimoto, to avoid wasting resin material. In addition, because Elenius, Hashimoto, and Matsumoto teach that different methods could be use to form the protective layer, it would have been obvious to one of ordinary skill in the art to substitute one method for the other to achieve the predictable result of protecting the second surface of the semiconductor element. *KSR International Co. v. Teleflex Inc.*, 550 U.S.--,82 USPQ2d 1385 (2007).

13. The prior art, however, fails to teach that the protective tape be a peelably removable UV sensitive tape wherein the hardened synthetic resin bonds the tape of the semiconductor element. Elenius, however, does teach that the protective layer is an epoxy layer (see, *e.g.*, col.8/ll.29). Yamada, on the other hand, teaches using an epoxy

layer **14** as the adhesive layer of a protective UV sensitive tape **15** to facilitate removing the tape without applying excessive stress to the semiconductor element (see, *e.g.*, col.1/ll.29-38,46-55).

14. Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art to have the tape of Elenius/Matsumoto/Hashimoto be a UV sensitive tape, as suggested by Yamada, to facilitate removing the tape without applying excessive stress to the semiconductor element.

15. Claims 12, 14-17, 19-22, 24-27, and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Elenius, Hashimoto, Matsumoto, and Yamada.

16. Regarding claim 12, AAPA shows (see, *e.g.*, fig. 4) most aspects of the instant invention including a semiconductor device comprising:

- A semiconductor element **100** having a first surface and a second surface opposite to the first surface
- An electrode **102** formed at the first surface of the semiconductor element **100**
- A wiring portion **104** formed on the first surface and connected to the electrode
- A conductive post **106** formed on the first surface and connected to the wiring portion **104**
- A resin layer **108** formed on the first surface so as to cover the first surface, the wiring portion **104**, and a side of the conductive post **106**
- An external connection **110** formed on the post **106**

Wherein:

- An end portion of the semiconductor element **14** is aligned with an end portion of the resin layer **32**
- The end portions of the semiconductor element **14**, and the resin layer **32** define an outer edge of the device

17. AAPA, however, fails to show a protective layer on the second surface of the semiconductor element, wherein the protective layer is aligned with the resin layer and the semiconductor element to define an outer edge of the device, and wherein the protective layer is a tape of a hardened synthetic resin achieving bonding function. Elenius, on the other hand, teaches that said protective layer would provide mechanical protection to the second surface of AAPA's semiconductor element (see, *e.g.*, col.8/ll.30-33).

18. It would have been obvious at the time of the invention to one of ordinary skill in the art to form the protective layer of Elenius on the second surface of AAPA's semiconductor element to provide mechanical protection to the second surface of the element.

19. Regarding claims 14, 19, 24, and 29, Elenius shows the protective layer comprises a polyimide or an epoxy resin (see, *e.g.*, col.8/ll.29).

20. Regarding claims 15, 20, 25, and 30, AAPA shows the external connection **110** is a solder ball (see, *e.g.*, fig. 4).

21. Regarding claims 16, 21, 26, and 31, AAPA shows the conductive post **106** is comprised of copper (see, *e.g.*, fig. 4).

22. Regarding claim 17, Elenius shows a side surface of the semiconductor element **14** is exposed from the resin layer **32** and the protective layer **34** (see, *e.g.*, fig. 2). See also the comments stated above in paragraphs 18-20 with respect to claim 12, which are considered repeated here.

23. Regarding claim 22, Elenius shows (see, *e.g.*, fig. 2):

- The conductive post (lower portion of **28**) having a first end portion and a second end portion
- The post being formed on the first surface
- The first end portion of the post being connected to the wiring portion **30**
- The second end portion of the post is not covered by the resin layer **32**
- The external connection **28** is formed on the second end portion of the post
- Only a side surface of the semiconductor element **14** is exposed from the resin layer **32** and the protective layer **34**

24. Regarding claim 22, see also the comments stated above in paragraphs 18-20 with respect to claim 12, which are considered repeated here.

25. Regarding claim 27, Elenius shows (see, *e.g.*, fig. 2):

- A side surface of the protective layer **34** is in a same plane with both a side surface of the semiconductor element **14** and a side surface of the resin layer **32**
- The side surfaces of the protective layer **34**, the semiconductor element **14**, and the resin layer **32** define an outer edge of the device

26. Regarding claim 27, see also the comments stated above in paragraphs 18-20 with respect to claim 12, which are considered repeated here.

27. Regarding claims 12, 17, 22, and 27, it is noted that Elenius shows most aspects of the claimed invention. He, however, fails to show that the protective layer is a tape. On the other hand, Elenius' protective layer is a hardened synthetic resin applied by known spin coating processes (see, *e.g.*, col.8/ll.24-37).

28. In a similar device to Elenius, Matsumoto forms a protective layer on the second surface of a semiconductor element to prevent cracking and chipping (see, *e.g.*, abstract). Said protective layer may be formed by either sticking an adhesive tape or spin coating (see, *e.g.*, paragraph 0015). Although both processes could be used, the protective layer is preferably formed from then adhesive tape to avoid wasting resin material (see, *e.g.*, Hashimoto: pp.12/ll.21-28).

29. Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art to tape the protective layer of Elenius to the second surface, as suggested by Matsumoto and Hashimoto, to avoid wasting resin material. In addition, because Elenius, Hashimoto, and Matsumoto teach that different methods could be use to form the protective layer, it would have been obvious to one of ordinary skill in the art to substitute one method for the other to achieve the predictable result of protecting the second surface of the semiconductor element. *KSR International Co. v. Teleflex Inc.*, 550 U.S.--,82 USPQ2d 1385 (2007).

30. The prior art, however, fails to teach that the protective tape be a peelably removable UV sensitive tape wherein the hardened synthetic resin bonds the tape of the semiconductor element. Elenius, however, teaches that the protective layer is an epoxy layer (see, *e.g.*, col.8/ll.29). Yamada, on the other hand, teaches using an epoxy

layer **14** as the adhesive layer of a protective UV sensitive tape **15** to facilitate removing the tape without applying excessive stress to the semiconductor element (see, *e.g.*, col.1/ll.29-38,46-55).

31. Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art to have the tape of AAPA/Elenius/Matsumoto/Hashimoto be a UV sensitive tape, as suggested by Yamada, to facilitate removing the tape without applying excessive stress to the semiconductor element.

Response to Arguments

32. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

33. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

34. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

35. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(571) 273-8300**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(571) 272-1716** and between the hours of 10:00 AM to 8:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.

37. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the

automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

38. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/678-796	2/2/2008
Other Documentation:	
Electronic Database(s): EAST (USPAT, EPO, JPO)	2/2/2008

/Marcos D. Pizarro/

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